ABSTRACT OF THE DISCLOSURE

In placement of 6-bit interconnection lines in parallel, for example, interconnection lines for three lower-order bits having a high signal change frequency and interconnection lines for three higher-order bits having a low signal change frequency are placed alternately, so that each interconnection line for a lower-order bit is sandwiched by interconnection lines for higher-order bits. With this layout, the interconnection lines for higher-order bits serve like shield lines for the interconnection lines for lower-order bits. This effectively suppresses increase in delay in signal propagation due to change of a signal propagating through an interconnection line for a lower-order bit and a signal propagating through an interconnection line for a higher-order bit to opposite phases, without increasing the area.